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PATENT APPLICATION

PATENT AND TRADEMARK OFFICE

BEFORE THE HONORABLE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Application of

Nobuaki HASHIMOTO

On Appeal from Group: 2827

Application No.: 09/615,503

Examiner: D. Graybill

Filed: July 13, 2000

Docket No.: 101929.02

For: SEMICONDUCTOR DEVICE, METHOD OF FABRICATING THE SAME, CIRCUIT BOARD, AND ELECTRONIC APPARATUS

APPEAL BRIEF TRANSMITTAL

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Respectfully submitted,

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BRIEF ON APPEAL

Appeal from Group 2827

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I. INTRODUCTION

This Appeal is from an Office Action mailed November 19, 2003, finally rejecting claims 1-9 and 12-20. No claims are allowed.

A. Real Party in Interest

The real party in interest for this Appeal is Seiko Epson Corporation, by way of Assignment recorded in the U.S. Patent and Trademark Office at reel 011258, frame 0349.

B. Statement of Related Appeals and Interferences

There are presently no appeals or interferences, known to Appellant, Appellant's representatives or the Assignee, which will directly effect or be directly effected by or have a bearing on the Board's decision in the pending Appeal.

C. Status of Claims

Claims 1-20 are pending. Claims 10 and 11 have been withdrawn. Claims 1-9 and 12-20 stand rejected and are on appeal. The claims on appeal are set forth in the attached Appendix. Claim 1 is independent. Claims 2-9 and 12-20 depend from claim 1.

D. Status of Amendments

A Request for Reconsideration was filed in the U.S. Patent and Trademark Office on February 5, 2004 in response to the November 19, 2003, Office Action. The Advisory Action mailed March 5, 2004 indicates that the Request for Reconsideration did not appear to overcome the rejections. All claim amendments have been entered of record.

II. SUMMARY OF THE INVENTION

A. Prior Art Problems Overcome by the Invention

To manufacture semiconductor devices, chips are assembled in packages by mounting on a substrate. Using a tape ball grid array (T-BGA) and tape automated bonding (TAB), semiconductor chips can be assembled continuously. In this method, a plurality of semiconductor chips are attached to a tape on a reel-to-reel transport system. In the related

art, external terminals are provided on the package and then the tape is cut to provide individual semiconductor chips. However, it is difficult to provide external terminals in a reel-to-reel transport system prior to cutting the tape. Furthermore, if a faulty sample occurs, there are large disposal losses.

B. General

The invention addresses these problems. Specifically, the invention provides a method to form external terminals on the film carrier tape and reduces losses caused by faulty samples. The method of claim 1 uses a reel to reel transport system to partially assemble a semiconductor device and then provide external terminals after the device is removed from the reel to reel transport system. Specifically, using a reel to reel transport system a plurality of semiconductor chips are attached to a tape. Then, continuing to use the reel to reel transport system, the tape is cut to obtain substrate. Then, the substrates are removed from the reel to reel transport system and external terminals are provided.

C. Embodiment of the Invention

1. Structure of the Invention

As shown in Fig. 6, a semiconductor device includes an insulating film 12 that is formed by punching a portion of a film carrier tape 30. The film carrier tape 30 is wound on a reel 33 as shown in Fig. 1a. A semiconductor chip 16 is mounted on the substrate 12 and external terminals 14 are formed on leads 20. Each external terminal 14 is made of a material, such as solder.

In the method to manufacture semiconductor device of the invention, a plurality of semiconductor chips 16 are attached to the film carrier tape 30, as shown in Figs. 1a and 1b. The film carrier tape 30 is wound on a reel 33. The end of the film carrier tape 30 is rolled out, and then rolled up by a take up reel 34. This is a reel-to-reel transport system. Semiconductor chip 16 is bonded to the film carrier tape 30 between the reels 33 and 34 using

a bonding jig 31. Semiconductor chips 16 are thus mounted on the film carrier tape successively. Then the reel 34 takes up the film carrier tape 30 having a plurality of semiconductor chips 16 mounted thereon.

Subsequently, the film carrier tape is wound on reel 37, as shown in Fig. 5. The reel is set on another fabrication device and the film carrier tape is unwound between reels 37 and 38. Individual substrates (insulating film 12) are punched out.

On each individual substrate external terminals 14 are formed. Then, for each piece of insulating film 12, tests are carried out. These tests include a visual mounting check and a test of electrical characteristics to obtain the finished product.

2. Advantage over the Prior Art

In the related art, a fabrication device is used to mount the external terminals as the film carrier tape is unwound between reels. In the invention, the external terminals 14 are provided using a general purpose device. This makes it easier to form the external terminals because position of external terminals in one type of product is usually different from that in another type of product. Accordingly, in a reel to reel transport system, a complicated controller may be required to correspond to the position of the external terminals depending on types of products, while a tape is reeled up in a different way, depending on a distance between any two adjacent semiconductor devices on the tape. Furthermore, the packages having the external terminals aren't wound on the reel, which may result in damage to the terminals.

In a general reel to reel transport system, a process of forming defective external terminals in one semiconductor device on a tape results in forming other defective external terminals in an adjacent semiconductor device on the same tape.

Because the present invention includes providing external terminals after cutting a tape, a process of forming defective external terminals does not affect formation of other external terminals in another semiconductor device, providing smaller disposal losses.

Finally, because it is easier to handle smaller packages, damage is less likely to occur after the external terminals are attached.

D. The Claimed Invention

1. Claim 1

Claim 1 recites a method of fabricating a semiconductor device comprising: attaching a plurality of semiconductor chips 16 to a tape 30, cutting the tape 30 to obtain substrate 12 after attaching the plurality of semiconductor chips 16, and providing a plurality of external terminals 14 on each of the substrates 12 after cutting the substrates. Attaching the plurality of semiconductor chips 16 to tape 30 and cutting tape 30 to obtain substrates 12 is carried out in a reel-to-reel transport system as shown in Figs. 1a and 5, respectively.

III. ISSUES AND REJECTIONS

The November 19, 2003 Office Action rejects claims 1-4, 9 and 12-20 under 35 U.S.C. §103(a) over U.S. Patent No. 5,905,633 to Shim (the 633 Patent) and claims 1-9 and 12-20 under 35 U.S.C. §103(a) over Shim in view of U.S. Patent No. 5,583,378 to Marrs (the 378 Patent).

The only issues on appeal are whether the subject matter of claim 1 would be obvious to one of ordinary skill in the art under 35 U.S.C. §103(a) over the 633 Patent and over the 633 Patent in view of the 378 Patent.

IV. GROUPING OF CLAIMS

Group 1 consists of claims 1-9 and 12-20. Claims 2-9 and 12-20 stand or fall with claim 1.

V. ARGUMENT

A. The Law

1. Law Regarding Factual Inquiries to Determine Obviousness/Non-Obviousness

Several basic factual inquiries must be made to determine obviousness or non-obviousness of patent application claims under 35 U.S.C. §103. These factual inquiries are set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966):

> Under §103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background, the obviousness or non-obviousness of the subject matter is determined.

The specific factual inquiries set forth in Graham have not been considered or properly applied by the Examiner in formulating the rejection of claims 3 and 12. Particularly, the differences between the prior art and the claims were not properly determined. As stated by the Federal Circuit in In re Ochiai, 37 USPQ2d 1127, 1131 (Fed. Cir. 1995):

> [t]he test of obviousness *vel non* is statutory. It requires that one compare the claim's subject matter as a whole with the prior art to which the subject matter pertains. 35 U.S.C. §103.
>
> The inquiry is thus highly fact-specific by design.... When the references cited by the Examiner fail to establish a *prima facie* case of obviousness, the rejection is improper and will be overturned. In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1956, 1598 (Fed. Cir. 1988). (Emphasis added).

In rejecting claims under 35 U.S.C. §103, an Examiner bears an initial burden of presenting a *prima facie* case of obviousness. A *prima facie* case of obviousness is established only if the teachings of the prior art would have suggested the claimed subject matter to a person of ordinary skill in the art. If an Examiner fails to establish a *prima facie* case, the rejection is improper and will be overturned. See In re Rijckaert, 9 F.3d 1531, 28

USPQ2d 1955 (Fed. Cir. 1993). "If examination... does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to the grant of the patent." In re Oetiker, 977 F.2d 1443, 1445-1446, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

B. Rejections Under 35 U.S.C. §103

1. Position Asserted in the November 19, 2003 Office Action

a. The November 19, 2003, Office Action rejects claims 1-4, 9 and 12-20 under 35 U.S.C. §103(a) over the 633 Patent. The Office Action recognizes that the 633 Patent does not "explicitly teach providing the plurality of external terminals on each of the substrates after the [cutting the tape to obtain substrates.]" None the less, the Office Action states "it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed sequence because applicant has not disclosed that the limitation is for a particular unobvious purpose, produces an unexpected result or is otherwise critical." "Moreover, it is well established that, in a well known process, the order of performing process steps is *prima facie* obvious in the absence of new or unexpected results." Ex parte Rubin, 129 USPQ 440 (Bd. App. 1959). (NOTE: The Office Action incorrectly cites Rubin. The proper citation is In re Burhans, 154 F.2d 690, 692, 69 USPQ 330, 332, (CCPA 1946). See MPEP §2144.04(IV)(c))

b. The Office Action also rejects claims 1-9 and 12-20 under 35 U.S.C. §103(a) over the 633 Patent in view of the 378 Patent. The Office Action recognizes that the 633 patent does not explicitly teach providing the plurality of external terminals on each of the substrate after cutting the tape to obtain substrates. The Office Action asserts that the 378 patent provides the deficiencies of the 633 patent by teaching providing a plurality of external terminals 218J on each of the substrates, 280G after the steps of attaching a plurality of

semiconductor chips 202H to a tape 299E and cutting the tape to obtain the substrate. The motivation to combine the references is that it would facilitate cost effective and efficient mass production.

2. The 633 Patent

The 633 Patent discloses BGA semiconductor packages which utilize a metal carrier frame 60 (64) to prevent thermal deformation of printed circuit boards (PCB) 10 during repeated high temperature processing steps. The metal carrier frame 60 (64) becomes a heat spreader for individual BGA packages. In fact, Shim teaches providing signal input and output solder balls prior to cutting a plurality of BGA's into individual packages. See e.g., col. 2, lines 30-35.

3. Claim 1 is Distinguishable Over the 633 Patent

A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

If the external terminals were provided after separating the carrier into individual BGA packages, it would partially eliminate the need for the metal carrier frame of the 633 Patent. This is because providing the external terminals is one of the processes that causes the thermal deformation the metal carrier prevents. Thus, providing the external terminals after cutting the carrier into individual BGA packages, teaches away from the purpose of the invention because the high temperature steps are spread out over the production process preventing the build up of temperatures in the package.

The Office Action asserts that claim 1 does not satisfy the requirements of Burhans (incorrectly cited as Rubin) which holds that "[I]t is well established that, in a well known

process, the order of performing steps is *prima facie* obvious in the absence of new or unexpected results." 154 F.2d 690, 692. (Emphasis added.) However, claim 1 does provide new results as compared to the 633 Patent.

Specifically, providing the external terminals after the tape is cut into substrates, makes it easier to provide the external terminals, as compared to providing them in a reel-to-reel transport system and reduces disposal losses. Thus, the requirements laid out in Burhans are satisfied.

The 633 Patent specifically discloses attaching the external terminals after cutting the substrate. See e.g., col. 2, lines 12-35. Although the Office Action states that it would have been an obvious matter of design choice to provide the external terminals after cutting the tape, the Office provides no motivation to do so.

4. The 378 Patent

The 378 Patent discloses an integrated circuit chip 202 having a thermal conductor 204. The thermal conductor 204 is applied to an interconnection substrate 208 and is linearly coextensive with inner connection substrate 208. Thermal conductor panel 204 and inner connection substrates 208 are formed into a panel of packaging that is 299E. Strips 280G are punched or routed out of panel 299E. Once strips 280G are created, integrated circuit chips 202H are attached. If solder balls 218J are required, they are applied to the package unit 270.

5. Claim 1 is Distinguishable Over the 633 Patent in View of the 378 Patent

Although the 378 Patent and the invention of claim 1 relate to ball grid array packages, claim 1 specifically recites that steps a and b are carried out in a reel-to-reel transport system. The 378 Patent merely discloses that the ball grid array packages can be produced in accordance with the invention by low cost methods through incorporation and utilization of machinery and infrastructure already existing in the integrated circuit packaging

and printed circuit board industries. See e.g., col. 6, lines 4-8. Thus, the 378 Patent does not recognize the problems that are solved by the invention. Specifically, the 378 Patent does not recognize that: 1) it is difficult to provide external terminals in a reel-to-reel transport system; and 2) by providing the external terminals after cutting the substrate, the disposal losses are less.

In determining the differences between the prior art and the claims, the question of 35 U.S.C. §103 is not whether the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious. MPEP 2141.02. Thus, because 378 Patent is not analogous as discussed above and is not concerned with a reel-to-reel transport system, it does not consider the invention of claim 1 as a whole.

Furthermore, as discussed above, the 633 Patent discloses a BGA semiconductor package that utilizes a metal carrier frame to prevent thermal deformation of printed circuit boards during repeated high temperature processing steps. If the external terminals are provided after separating the carriers into individual BGA packages, as in the 378 Patent, it would eliminate the need for the metal carrier frame because providing external terminals is one of the repeated processes that causes the thermal deformation the metal carrier prevents. Thus, the feature of the 378 Patent of applying the external terminals after cutting the substrate, teaches away from the 633 Patent.

VI. CONCLUSION

For at least the reasons discussed above, it is respectfully submitted that the claims are distinguishable over the 633 Patent under 35 U.S.C. §103 and are distinguishable over the 633 Patent in view of the 378 Patent under 35 U.S.C. §103.

For the above reasons, Applicant respectfully requests this honorable board to reverse the rejection of the claims.

Respectfully submitted,

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Date: May 19, 2004

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APPENDIX A

CLAIMS:

1. A method of fabricating a semiconductor device comprising:

(a) attaching a plurality of semiconductor chips to a tape;

(b) cutting the tape to obtain substrates after the step (a); and

(c) providing a plurality of external terminals on each of the substrates after the step (b),

wherein the steps (a) and (b) are carried out in a reel-to-reel transport system.

2. The method of fabricating a semiconductor device as defined in claim 1, further comprising:

attaching a reinforcing member to the tape in positions corresponding to each of the semiconductor chips, before the step (b).

3. The method of fabricating a semiconductor device as defined in claim 1,

wherein the tape is cut into regions each including one of the semiconductor chips in the step (b).

4. The method of fabricating a semiconductor device as defined in claim 2,

wherein the tape is cut into regions each including one of the semiconductor chips in the step (b).

5. The method of fabricating a semiconductor device as defined in claim 1,

wherein the tape is cut into regions each including two or more of the semiconductor chips in the step (b).

6. The method of fabricating a semiconductor device as defined in claim 2,

wherein the tape is cut into regions each including two or more of the semiconductor chips in the step (b).

7. The method of fabricating a semiconductor device as defined in claim 5, further comprising:

cutting each of the substrates into regions, each including one of the semiconductor chips, after the step (c).

8. The method of fabricating a semiconductor device as defined in claim 6, further comprising:

cutting each of the substrates into regions, each including one of the semiconductor chips, after the step (c).

9. The method of fabricating a semiconductor device as defined in claim 1,

wherein a plurality of device holes are formed in the tape, and leads are formed on the tape, which end portions project into the respective device holes; and

wherein each of the semiconductor chips is disposed within a respective one of the device holes, and the electrodes of the semiconductor chips and the leads are bonded in the step (a).

10. (Withdrawn)

11. (Withdrawn)

12. The method of fabricating a semiconductor device as defined in claim 1,

wherein each of the semiconductor chips is bonded to the tape in a face-up configuration in the step (a).

13. The method of fabricating a semiconductor device as defined in claim 12,

wherein the electrodes of the semiconductor chips and leads formed on the tape are electrically connected by means of wires in the step (a).

14. The method of fabricating a semiconductor device as defined in claim 1, further comprising:

attaching a heat radiating member to each of the semiconductor chips.

15. The method of fabricating a semiconductor device as defined in claim 2, further comprising:

attaching a heat radiating member to each of the semiconductor chips.

16. The method of fabricating a semiconductor device as defined in claim 1, further comprising:

attaching the heat radiating member before the step (b), with a reel-to-reel transport system.

17. The method of fabricating a semiconductor device as defined in claim 2, further comprising:

attaching the heat radiating member before the step (b), with a reel-to-reel transport system.

18. A semiconductor device fabricated by the method as defined in claim 1.

19. A circuit board having mounted the semiconductor device as defined in claim 18.

20. An electronic apparatus including the semiconductor device as defined in claim 18.